a transfer gate transistor coupled to the pull-down transistor and including a second gate having a second width and including a second gate insulator having a second thickness, a product of the first width and the second thickness being greater than or equal to a product of the second width and the first thickness.

22. A memory cell, comprising:

a pull-down transistor including a first channel region having a first width and including a first gate insulator having a first thickness; and

a transfer gate transistor including a second channel region having a second width and including a second gate insulator having a second thickness, a product of the first width and the second thickness being greater than or equal to a product of the second width and the first thickness.

REMARKS

Claims 1 – 22 are pending in this broadening reissue application.

The Applicants have amended claims 1, 4, 6, and 9 and have added new circuit claims 13 – 20 and new memory-cell claims 21 – 22 to broaden the scope of protection to their invention. The Applicants have also amended the drawings and specification to correct typographical errors.

The Applicants have added no new matter to the reissue application.

In light of the foregoing, original claims 2 – 3, 5, 7 – 8, and 10 - 12 as issued, claims 1, 4, 6, and 9 as amended, and new claims 13 – 22 are in condition for full allowance, and that action is respectfully requested.